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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/554,139	02/01/2008	Sherif Ahmed Hammouda	1011-72254-01	3186

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EXAMINER	
LIN, SUN J	

ART UNIT	PAPER NUMBER
2825	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/554,139	HAMMOUDA ET AL.	
	Examiner	Art Unit	
	Sun J. Lin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,11,13-15,17 and 18* is/are rejected.

7)☒ Claim(s) *9,12 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 February 2008* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/20/05,9/29/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/554,139 filed on 02/01/2008. Claims 1 – 18 remain pending in the application.

Claim Objections

2. Claims listed below are objected to because of the following informalities:

Claim 1, line 5, before "device level" delete –-**the**–.
Claim 1, line 6, before "circuit" insert —**analog**—.
Claim 1, line 6, change "the analysis" to —**results of the analyzing**–.
Claim 2, line 1, before "analyzing" insert –-**the**–.
Claim 2, line 1 – 2, before "device level" delete —**the**—.
Claim 2, line 2, change "includes" to –-**comprises**–.
Claim 2, line 2, before "circuit" insert —**analog**—.
Claim 2, line 2 – 3, before "resizing" delete —**the**—.
Claim 2, line 3, before "based" delete —**is**—.
Claim 2, line 3, before "mode of operation" insert –-**determined**—.
Claim 3, line 1, before "analyzing" insert –-**the**–.
Claim 3, line 1 – 2, before "device level" delete —**the**—.
Claim 3, line 2, change "includes" to –-**comprises**–.
Claim 3, line 2, before "resizing" delete –-**the**–.
Claim 3, line 3, before "based" delete —**is**—.
Claim 4, line 1, before "analyzing" insert –-**the**–.
Claim 4, line 1 – 2, before "device level" delete —**the**—.
Claim 4, line 2, change "includes" to –-**comprises**–.
Claim 4, line 6, change "the results" to –-**analysis results**–.
Claim 5, line 1, before "analyzing" insert –-**the**–.
Claim 5, line 1 – 2, before "device level" delete —**the**—.
Claim 5, line 2, change "includes" to –-**comprises**–.
Claim 6, line 1, change "including" to –-**comprising**—.
Claim 7, line 1, after "claim 1," insert —**further comprising**—.
Claim 7, line 1 – 2, delete —**identifying circuit blocks within the analogy circuit;**—.

Claim 7, before line 3, insert — **identifying circuit blocks within the analogy circuit;**—.

Claim 7, line 3, before "circuit blocks" insert —**the**—.

Claim 7, line 4, before "transistor" delete —**next**—.

Claim 7, line 4, change "circuit block" to —**circuit blocks**—.

Claim 8, line 1, before "analyzing" insert —**wherein the**—.

Claim 8, line 1, change "includes" to —**comprises**—.

Claim 9, line 1, change "including" to —**comprising**—.

Claim 9, line 2, before "description" insert —**circuit**—.

Claim 9, line 3, change "the resized results" to —**results of the resizing**—.

Claim 10, line 1, change "claim 1" to —**claim 2**—.

Claim 10,line 1, before "a transistor" delete —**of**—.

Claim 10, line 1, change "includes" to —**comprises**—.

Claim 10, line 2, before "output conductance" delete —**the**—.

Claim 10, line 3, before "transistor" insert —**resized**—.

Claim 12, line 1, change "including" to —**comprising**—.

Claim 13, line 1, change "including" to —**comprising**—.

Claim 13, line 3, change "including" to —**comprising**—.

Claim 14, line 1, change "including" to —**comprising**—.

Claim 15, line 1, change "including" to —**comprising**—.

Claim 15, line 3, change "including" to —**comprising**—.

Claim 15, line 3, before "retargeting system" insert —**circuit**—.

Claim 16, line 1, change "claim 11" to —**claim 15**—.

Claim 17, line 1, before "circuit" insert —**analog**—.

Claim 18, line 5, before "device level" delete —**the**—.

Claim 18, line 6, change "the analysis" to —**results of the analyzing**—.

Appropriate corrections are required.

Claim Rejections - 35 USC § 101

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 101 that form the basis for the rejections under this section made in this Office action:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title. *Also, based on Supreme Court precedent and recent Federal Circuit decisions, to*

quality as a § 101 statutory process, the claim should (1) be tied to another statutory class (a particular machine or apparatus) or (2) transform underlying subject matter (such as an article or materials) to a different state or thing.

4. Claims 1 – 8 and 10 are rejected under 35 U.S.C. 101 because none of method steps of the claimed invention is tied to another statutory class (a particular machine or apparatus).

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6 Claims 1 – 3, 5 – 8, 11, 13, 17 and 18 are rejected under 35 U.S.C. 102(b) as being unpatentable over a technical article entitled "A Fully Automated Approach for Analog Circuit Reuse" authored by *Hammouda et al.*

7. As to Claim 1, *Hammouda et al.* show and disclose the following subject matter:

- Analog circuit reuse... A method/system for converting an analog circuit to from a source technology to a target technology ("technique for automated analog circuit resizing between different technologies") – [title; abstract; Fig. 1];
- IP portion (i.e., analog circuit) reuse in different technologies – [abstract]; Analog design reuse – [Paragraph 3, line 1 – 6]; Receiving the analog circuit in the source technology – [page 1, col. 2, last paragraph; Fig. 1];
- Converting the analogy circuit from the source technology to the target technology ("map *reuse analog IP* to a different target technology" – page 1, col. 2, last paragraph) by analyzing the analogy circuit *at device level* ("*hierarchy of the design is the first thing extracted, then all device dimensions, currents, biasing voltages, parasitics associated with the devices as well as symmetry information is extracted from each device in each subcircuit in the design*" – page 2, col. 1, line 3 – 7) based on the analysis

("preserve the characteristics of each device between source technology and target technology" – page 2, col. 1, line 8 – 9); and

- Outputting the analog circuit in the target technology ("output of the circuit-sizing engine is a new spice netlist – page 1, col.1, last paragraph, Fig. 1].

For reference purposes, the explanations given above in response to Claim 1 are called **[Response A]** hereinafter.

8. As to Claim 18, reasons are included in **[Response A]** given above.

9. As to Claim 2, in addition to reasons included in **[Response A]** given above, *Hammouda et al.* disclose analyzing the analog circuit at device level comprises determining *region of operation* (i.e., *mode of operation*) for a transistor in the analog circuit and resizing of the transistor based on the determined mode of operation – [page 2, col. 1, line 7 – 11, line 26 – 30].

10. As to Claim 3, in addition to reasons included in **[Response A]** given above, *Hammouda et al.* disclose analyzing the analog circuit at device level comprises determining *node voltages* coupled to a device and resizing the device based on the *determined node voltages* – [page 2, col. 1, line 7 – 11, line 26 – 30].

11. As to Claim 5, in **[Response A]** given above, *Hammouda et al.* disclose analyzing the analog circuit at device level comprises analyzing device level dimensions of individual devices, *Hammouda et al.* also disclose analyzing transistor dimensions in individual electrical devices need to be analyzed – [page 2, col. 1, line 19 – 30].

12. As to Claim 6, in addition to reasons included in **[Response A]** given above, *Hammouda et al.* disclose following subject matter:

- Design extraction – extracting (DC) biasing voltages from *each device* in *each subcircuit* in the analog design under study – [page 2, col. 1, line 3 – 11];
- The design extraction engine extracts all necessary data (i.e., electrical parameters) using a Full spice simulator – [Fig. 1; page 2, col. 1, 19 – 22];

noted that the *full spice simulator* performs a *dc simulation of the analog circuit in the source technology to determine electrical parameters (e.g., biasing voltages) of devices in the analogy circuit under study* – [Fig. 1; page 2, col. 1, 19 – 22];

- Netlist migration – resizing is based on the determined electrical parameters determined by design extraction engine – [Fig. 1].

For reference purposes, the explanations given above in response to Claim 6 are called **[Response B]** hereinafter.

13. As to Claim 7, *Hammouda et al.* disclose the subject matter (block recognition engine...extracting different basic building blocks inside the analog design...(resizing) transistor dimensions in target technology – [Fig. 1; page 2, col. 1, line 22 – 30].

14. As to Claim 8, *Hammouda et al.* disclose preserving of each device between source technology and target technology by changing the dimensions (sizes of resistors) of the devices and *scaling* the current and *node voltages* – [page 2, col. 1, line 7 – 11]; Noted that node voltages are coupled to a biasing resistor, which is resized based on scaling factor of the node voltages.

15. As to Claim 11, reasons are included in **[Response A]** and **[Response B]** given above. Noted that *Hammouda et al.* disclose a circuit retargeting system in Fig 1, wherein design extraction is performed by a design extraction engine, and netlist migration is performed by a resizing engine.

16. As to Claim 13, *Hammouda et al.* disclose the subject matter in Fig.1 and explained in **[Response B]** given above.

17. As to Claim 17, *Hammouda et al.* disclose the subject matter – [page 2, col. 1, line 11 – 15].

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

(1). Determining the scope and contents of the prior art.
(2). Ascertaining the differences between the prior art and the claims at issue.
(3). Resolving the level of ordinary skill in the pertinent art.
(4). Considering objective evidence present in the application indicating obviousness or nonobviousness.

19. Claims 10 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over a technical article entitled “A Fully Automated Approach for Analog Circuit Reuse” authored by *Hammouda et al.* in view of a technical article entitled “Analog IP Design Retargeting based on Design Extraction and Transistor Optimization” authored by *Dessouky et al.*

20. As to Claim 10, *Hammouda et al.* disclose resizing a transistor in an analog circuit, they do not teach a method of checking that changes to output conductance and parasitic capacitance of the resized transistor remain within a certain accuracy limit. But *Dessouky et al.* teach this method – [page 9, line 15 – 22]. *Dessouky et al.* disclose checking changes to output conductance and parasitic capacitance of resized transistor remain within a certain accuracy limit in order to achieve identical liner performance.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teaching of *Dessouky et al.* in checking changes to output conductance and parasitic capacitance of resized transistor remain within a certain accuracy limit in order to achieve identical liner performance.

21. As to Claim 14, *Hammouda et al.* disclose using a resizing engine in a circuit retargeting system; they do not expletively teach a method of coupling a source technology parameter database and a target technology parameter database to the resizing engine. But *Dessouky et al.* disclose this method – [Fig. 3]. *Dessouky et al.* teach coupling a source technology parameter database and a target technology parameter database to the resizing engine in order to provide retargeting algorithm with sufficient information thereby deducing accurate target netlist.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teaching of *Dessouky et al.* in coupling a source technology parameter database and a target technology parameter database to the resizing engine in order to provide retargeting algorithm with sufficient information thereby deducing accurate target netlist.

22. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over a technical article entitled "A Fully Automated Approach for Analog Circuit Reuse" authored by *Hammouda et al.* in view of U.S. Patent Application Publication No. 2007/0033550 A1 to *Berger et al.*

23. As to Claim 15, *Hammouda et al.* disclose a circuit retargeting system. They do not teach a method of distributing the retarget system by coupling a client computer and a server computer through a network. But *Berger et al.* teach this method. *Berger et al.* disclose the following subject matter:

- (Circuit) Migration engine (i.e., circuit retargeting system) – [Fig. 1; Fig. 2];
- Migration processor comprises a general-purpose computer...programmed in software to carry out functions of circuit migration...software may be *downloaded* to the (client) computer (from a server computer) over a ***Network*** – [Paragraph 0050].

Noted that the purpose of distributing the retarget system by coupling a server computer and a client computer through a network is to allow many engineers (i.e., internal clients), with a permission, to access the software to perform circuit migration.

Therefore, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to have applied the teaching of *Berger et al.* in coupling a (internal) client computer, with a permission, and a server computer through a network in order to download software necessary for circuit migration.

Allowable Subject Matter

24. Claims 9, 12 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Those claims are allowed is because that the prior art does not teach or fairly suggest the following subject matter:

- A method of converting an analog circuit from a source technology to a target technology, the method comprising: *receiving, on a server computer, a circuit description from a client computer over a distributed network, resizing the circuit description on the server, and* ***returning results of the resizing*** *to the client computer over the distributed circuit* in combination with other limitations recited in **Claim 9**;
- A circuit retargeting system to convert an analog circuit from a source technology to a target technology, the circuit retargeting system comprising *an optimization engine coupled to a resizing engine, the optimization engine changes a resized analog circuit by taking into account timing issues and constraints* in combination with other limitations recited in **Claim 12**;
- A circuit retargeting system to convert an analog circuit from a source technology to a target technology, the circuit retargeting system comprising *a server computer receives the analogy circuit in the source technology, resizes the analog circuit to the target technology, and sends the resized analog circuit to a client computer through a network* in combination with other limitations recited in **Claim 16**.

Examiner's Remark

25. Claim 4, currently being rejected per *35 USC § 101* due to reasons given above, has allowable subject matter. Allowability of Claim 4 is pending on amendment of its parent claim (i.e., Claim 1) to overcome 101 issue mentioned above.

Conclusion

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to *Sun James Lin* whose telephone number is (571) 272 - 1899. The examiner can normally be reached on Monday-Friday 9:30AM - 6:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, *Jack Chiang* can be reached on (571) 272 - 7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free) If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (in USA or CANADA) or 571-272-1000.

All responses to this Office Action should be mailed to ***Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450*** or faxed to ***571-273-8300***.

/Sun J Lin/
Primary Examiner, Art Unit 2825